The claims:

1. A method for fabrication of a semiconductor device, the semiconductor device having a plurality of epitaxial layers on a substrate, the plurality of epitaxial layers including an active region in which light is able to be generated; the method comprising:
   (a) applying at least one first ohmic contact layer to a front surface of the epitaxial layer, the first ohmic contact layer also acting as a reflector;
   (b) removing the substrate from a rear surface of the epitaxial layers; and
   (c) texturing the rear surface.

2. A method as claimed in claim 1, wherein before the substrate is removed a relatively thick layer of the thermally conductive metal is electroplated on the reflector layer.

3. A method as claimed in claim 1 or claim 2, wherein before the substrate is removed, a seed layer of a thermally conductive metal is applied to the ohmic contact layer, and a relatively thick layer of the thermally conductive metal is electroplated on the seed layer.

4. A method as claimed in claim 3, wherein the front surface is coated prior to application of the seed layer, the coating being one or more of: an adhesion layer, and a multiple layer stack.

5. A method as claimed in claim 3 or claim 4, wherein a patterned layer is added to the seed layer before the electroplating step, and the electroplating of the relatively thick layer is between the patterns.

6. A method as claimed in claim 5, wherein the patterned layer comprises photoresist patterns.

7. A method as claimed in claim 3 or claim 4, wherein the seed layer is patterned before the electroplating step, and the electroplating of the relatively thick layer is between the patterns.

8. A method as claimed in claim 7, wherein the pattern on the seed layer comprises photoresist patterns.

9. A method as claimed in any one of claims 5 to 8, wherein the patterns are of a height in the range 3 to 500 micrometers.

10. A method as claimed in any one of claims 5 to 9, wherein the patterns have a thickness in the range 3 to 500 micrometers.

11. A method as claimed in any one of claims 5 to 10, wherein the patterns have a spacing in the range of 200 to 2,000 microns.

12. A method as claimed in any one of claims 3 to 6, wherein the seed layer is electroplated without patterning, patterning being performed subsequently.

13. A method as claimed in claim 12, wherein patterning is by photoresist patterning and then wet etching.

14. A method as claimed in claim 12, wherein patterning is by laser beam micro-machining of the relatively thick layer.

15. A method as claimed in any one of claims 1 to 14, wherein before removing the substrate annealing is performed to improve adhesion

16. A method as claimed in any one of claims 2 to 15, wherein the relatively thick layer is of a height no greater that the photoresist height.

17. A method as claimed in any one of claims 2 to 16, wherein the relatively thick layer of thermally conductive metal is electroplated to a height greater than the photoresist and is subsequently thinned.

18. A method as claimed in claim 17, wherein thinning is by polishing or wet etching.

19. A method as claimed in any one of claims 1 to 18, wherein the texturing step (c) is by at least one method selected from the group consisting of:

(a) patterning the rear surface and then etching,

(b) photolithography followed by deposition of a layer on the rear surface and then lift-off, and

(c) by depositing a thin metal film on the rear surface and then rapid thermal annealing of the metal to form a cluster of metal drops that is used as an etching mask for the texturing.

20. A method as claimed in claim 19, wherein etching is by one or more of the methods selected from the group consisting of: dry etching, wet etching, photochemical etching, and laser etching.

21. A method as claimed in any one of claims 1 to 20, wherein the texturing is of a shape and dimensions able to be varied.

22. A method as claimed in any one of claims 1 to 21, wherein after removing the substrate in step (b), the rear surface is etched and the rear surface is then textured.

23. A method as claimed in any one of claims 1 to 23, wherein after the substrate is removed in step (b), at least one layer added to the rear surface and the at least one layer is textured.

24. A method as claimed in any one of claims 1 to 23, wherein there is included an extra step of forming a second ohmic contact layer on the rear surface, the second ohmic contact layer being selected from the group consisting of: opaque, transparent, and semi-transparent, the extra step being performed at one of: after step (c), and between steps (b) and (c).

25. A method as claimed in claim 24, wherein the second ohmic contact layer is one of blank and patterned.

26. A method as claimed in claim 24 or claim 25, wherein bonding pads are formed on the second ohmic contact layer.

27. A method as claimed in any one of claims 2 to 23, wherein after the relatively thick layer is applied, ohmic contact formation and subsequent process steps are carried out, the subsequent process steps including deposition of wire bond pads.

28. A method as claimed in any one of claims 24 to 26, wherein the exposed second surface is cleaned and etched before the second ohmic contact layer is deposited.

29. A method as claimed in any one of claims 24 to 28, wherein the second ohmic contact layer does not cover the whole area of the rear surface.

30. A method as claimed in any one of claims 24 to 28, wherein if the second ohmic contact layer covers large portion of the rear surface, step (c) is performed directly on the second ohmic contact layer and the second ohmic contact layer is the textured surface.

31. A method as claimed in any one of claims 24 to 30, wherein there is included the step of separation into individual devices.

32. A method as claimed in any one of claims 1 to 31, wherein the semiconductor devices are fabricated without one or more selected from the group consisting of: lapping, polishing and dicing.

33. A method as claimed in any one of claims 1 to 32, wherein the at least one first ohmic contact layer is on p-type layers of the epitaxial layers.

34. A method as claimed in any claim 31, wherein the second ohmic contact layer is formed on n-type layers of the expitaxial layers.

35. A method as claimed in any one of claims 1 to 23, wherein after step (c), dielectric films are deposited on the epitaxial layers and openings are cut in the dielectric films and second ohmic contact layer, and bond pads deposited on the epitaxial layers.

36. A method as claimed in any one of claims 1 to 23, wherein after step (c), electroplating of a thermally conductive metal on the epitaxial layers is performed.

37. A method as claimed in any one of claims 33 to 36, wherein the thermally conductive metal comprises copper and the epitaxial layers comprise multiple GaN-related layers.

38. A method as claimed in 35, wherein step (c) is performed in the deposited dielectric film(s) instead of the rear surface.

39. A method for fabrication of a semiconductor device, the semiconductor device having a plurality of epitaxial layers on a substrate, the plurality of epitaxial layers including an active region in which light is able to be generated; the method comprising:

(a) patterning the substrate prior to the deposition of the plurality of epitaxial layers on the substrate;

(b) applying at least one first ohmic contact layer to a front surface of the plurality of epitaxial layers, the first ohmic contact layer also acting as a reflector; and

(c) removing the substrate from a rear surface of the epitaxial layers such that after the removal of the substrate, the rear surface is already patterned.

40. A method as claimed in claim 39, wherein after removal of the substrate no subsequent rear surface texturing is required.

41. A method for fabrication of a semiconductor device, the semiconductor device having a plurality of epitaxial layers on a substrate, the plurality of epitaxial layers including an active region in which light is able to be generated; the method comprising:

(a) patterning the plurality of epitaxial layers below the active region during the deposition of the plurality of epitaxial layers;

(b) applying at least one first ohmic contact layer to a front surface of the plurality of epitaxial layers, the first ohmic contact layer also acting as a reflector; and

(c) removing the substrate.

42. A method for fabrication of a semiconductor device, the semiconductor device having a plurality of epitaxial layers on a substrate, the plurality of

epitaxial layers including an active region in which light is able to be generated; the method comprising:

(a) applying at least one first ohmic contact layer to a front surface of the epitaxial layer, the first ohmic contact layer also acting as a reflector;

(b) removing the substrate from a rear surface of the epitaxial layers;

(c) depositing dielectric films on the epitaxial layers; and

(d) texturing the dielectric films.

43. A semiconductor device comprising epitaxial layers, first ohmic contact layers on a front surface of the epitaxial layers and providing a reflective surface, and a second ohmic contact layer on a rear surface of the epitaxial layers; the rear surface being surface textured.

44. A semiconductor device as claimed in claim 43, further comprising a relatively thick layer of a thermally conductive metal on the first ohmic contact layer, there being an adhesive layer on the first ohmic contact layer between the first ohmic contact layer and the relatively thick layer.

45. A semiconductor device as claimed in claim 44, wherein there is a seed layer of the thermally conductive metal applied to the adhesive layer.

46. A semiconductor device as claimed in any one of claims 43 to 45, wherein the relatively thick layer is at least 20 micrometers thick.

47. A semiconductor device as claimed in any one of claims 43 to 46, wherein the second ohmic contact layer is a thin layer in the range of from 3 to 500 nanometers.

48. A semiconductor device as claimed in any one of claims 43 to 47, wherein the second ohmic contact layer is selected from the group consisting of: opaque, transparent, and semi-transparent.

49. A semiconductor device as claimed in any one of claims 43 to 48, wherein the second ohmic layer includes bonding pads.

50. A semiconductor device as claimed in any one of claims 43 to 49, wherein the thermally conductive metal is copper and the epitaxial layers comprise multiple GaN-related epitaxial layers.

51. A semiconductor device as claimed in any one of claims 43 to 50, wherein the semiconductor device is selected from the group consisting of: a light emitting device, and a transistor device.

52. A semiconductor device as claimed in any one of claims 43 to 51, wherein the second ohmic contact layer is selected from the group consisting of: blank, and patterned.

53. A semiconductor device fabricated by the method of any one of claims 1 to 42.